ARGUMENTS/REMARKS

Claims 1-16, 41-50, and 66-85 are pending in the application. The Applicants' attorney has amended claims 1, 6, 8, 41, 43, 68, 71, 72, 74, 75, 76, 78, 79, 81, 82, 84, and 85. **If after considering this response the Examiner does not allow all of the claims, then the Applicants' attorney requests that the Examiner contact him to schedule and attend a telephone interview before issuing a subsequent Office Action.**

Objections To The Specification

The Applicants' attorney has amended the title for a second time to overcome this objection, and thus requests the Examiner to withdraw this objection.

Claim Objections

As requested by the Examiner, the Applicants' attorney has amended claims 6 and 8 to overcome this rejection, and thus requests the Examiner to withdraw this rejection.

Allowable Subject Matter

The Examiner is thanked for his careful examination of this application and the indication of allowable subject matter. Accordingly, dependent claims 68, 71, 72, 74-76, 78, 79, 81, 82, 84, and 85 have been rewritten in independent form.

Rejection Of Claims 1, 4-6, 41-43, 66, 80, and 83 Under 35 U.S.C. § 102(b) As Being Anticipated By U.S. Patent 5,909,565 to Morikawa et al. ("Morikawa")

The Applicants' attorney requests that the Examiner withdraw this rejection for the reasons set forth below.

Claim 1

Claim 1, as amended, recites a hardwired-pipeline circuit operable to receive, via a single bus, a message that includes data and that includes a header having information indicating a destination of the data, and to extract the data from the message.

For example, referring, *e.g.*, to FIGS. 4-5 and paragraphs [57] and [97] – [100] of the patent application, in one embodiment, a pipeline circuit 80 (FIG. 4) has an input-data handler 120 (FIG. 5) operable to receive via a single pipeline bus 50 (See also FIG. 3) a message that includes data and that includes a header having information indicating a destination pipeline 74 for the data, to extract the data from the message, and to load the extracted data into a memory 92. An interface 140 is operable to retrieve the extracted data from the memory 92, and the destination pipeline 74 is operable to process the retrieved data.

In contrast, Morikawa does not disclose a hardwired-pipeline circuit operable to receive, via a single bus, a message that includes data. Referring, *e.g.*, to FIG. 1 of Morikawa, a coprocessor 102 receives an instruction via a first bus (*i.e.*, a bus 126), receives data via a second bus (*i.e.*, a bus 124), and processes the received data beginning with a first coprocessing unit 150. Neither the data nor the instruction includes a header. Similar analyses apply to the coprocessors 202 (FIG. 4) and 302 (FIG. 10) of Morikawa. Thus, Morikawa does not disclose or fairly suggest a hardwired-pipeline circuit operable to receive, via a single bus, a message as recited in claim 1 and, instead, teaches that two separate buses are required.

Claims 4 and 5

These claims are patentable by virtue of their respective dependencies from claim 1.

Claim 6

Claim 6, as amended, recites a processor operable to broadcast a message that includes data and that includes a header having information indicating a destination of the data, and a hardwired-pipeline circuit operable to receive, via a single data stream, the message from the processor and to extract the data from the message.

For example, referring, *e.g.*, to FIGS. 3-5 and paragraphs [57] and [95] – [100] of the patent application, in one embodiment, a host processor 42 (FIG. 3) is operable to broadcast on a pipeline bus 50 a message that includes data and that includes a header having information indicating a destination of the data. A pipeline circuit 80 (FIG. 4) has an input-data handler 120 (FIG. 5) operable to receive, via a single data stream, the message from the bus 50, to extract the data from the message, and to load the extracted data into a memory 92. An interface 140 is operable to retrieve the extracted data from the memory 92, and the destination pipeline 74 is operable to process the retrieved data.

In contrast, Morikawa does not disclose a hardwired-pipeline circuit operable to receive, via a single data stream, a message from a processor. Referring, *e.g.*, to FIG. 1 of Morikawa, a coprocessor 102 receives an instruction via a first bus (*i.e.,* a bus 126), receives data via a second bus (*i.e.,* a bus 124), and processes the received data beginning with a first coprocessing unit 150. Neither the data nor the instruction includes a header. Thus, Morikawa teaches that instructions are provided to the coprocessor 102 via bus 126 and data is provided to the coprocessor 102 via bus 124 in separate data streams. Similar analyses apply to the coprocessors 202 (FIG. 4) and 302 (FIG. 10) of Morikawa. Thus, Morikawa does not disclose or fairly suggest a hardwired-pipeline circuit operable to receive, via a single data stream, a message as recited in claim 6.

Claim 41

Claim 41, as amended, recites receiving a message that includes data and that includes a header having information indicating a destination of the data and having information indicating a size of the message.

Morikawa does not disclose or fairly suggest the act of receiving a message that includes a header having information indicating a size of the message recited in claim 41.

Claim 42

This claim is patentable by virtue of depending from claim 41.

Claim 43

Claim 43 is patentable because Morikawa does not disclose or fairly suggest providing a message to an external source via a single bus.

Claim 66

This claim is patentable by virtue of depending from claim 1.

Claim 80

This claim is patentable by virtue of depending from claim 41.

Claim 83

This claim is patentable by virtue of depending from claims 43.

Rejection Of Claims 1, 4, 41-42, 66, And 80 Under 35 U.S.C. § 102(b) As Being Anticipated By Hennessy and Patterson, "Computer Architecture – A Quantitative Approach, 2nd, Edition," 1996

The Applicants' attorney requests that the Examiner withdraw this rejection for the reasons set forth below.

Claim 1

Claim 1 as amended recites a hardwired-pipeline circuit operable to receive, via a single bus, a message that includes data and that includes a header having information indicating a destination of the data, and to extract the data from the message.

In contrast, Hennessy discloses that a register receives instructions via a first bus and data from the data memory via a second bus. The value B appears to be the address of the data in the data memory. Thus, Hennessy does not disclose a

hardwired-pipeline circuit operable to receive a message via a single bus and, instead requires two separate buses.

Claim 4

Claim 4 is patentable by virtue of its dependency from claim 1.

Claim 41

Claim 41 as amended is patentable for reasons similar to those discussed above in support of the patentability of claim 1 over Hennessy. Additionally, Hennessy does not disclose receiving a message that includes data and a header having information indicating a size of the message.

Claim 42

This claim is patentable by virtue of depending from claim 41.

Claim 66

This claim is patentable by virtue of depending from claim 1.

Claim 80

This claim is patentable by virtue of depending from claim 41.

Rejection Of Claims 7-10, 44-45, 49, 69-70, And 73 Under 35 U.S.C. § 103(a) As Being Obvious In View of Morikawa

The Applicants' attorney requests that the Examiner withdraw this rejection for the reasons set forth below.

Claim 7

Claim 7 recites a hardwired-pipeline circuit operable to receive and process data, generate a message header that includes information indicating a destination of the processed data, generate a message that includes the processed data and the header, and provide the message to an external source.

For example, referring, *e.g.*, to FIGS. 4-5 and paragraphs [57] and [97] – [104] of the patent application, in one embodiment, a pipeline circuit 80 (FIG. 4) includes pipelines 74 that are operable to receive and process data. The pipeline circuit 80 also

includes an output-data handler 126 (FIG. 5) operable to generate a message header that includes information indicating a destination (*e.g.*, a thread of a software application running on the host processor 42 of FIG. 3) of the processed data, to generate a message that includes the processed data and the header, and to provide the message to an external source (*e.g.*, the host processor 42).

In contrast, Morikawa does not teach or suggest a hardwired-pipeline circuit operable to generate a message header that includes information indicating a destination of processed data, to generate a message that includes the processed data and the header, and to provide the message to an external source. Referring, *e.g.*, to Morikawa's FIG. 4, a coprocessor 202 receives data via a bus 124, and processes the received data with a coprocessor unit 211. Then, the coprocessor 102 provides the data to the processor 201 via a bus 125, and may provide control information to the processor via the bus 242. But the control information does not indicate a destination of the processed data, because an instruction executed by the processor 201 provides the destination; consequently, the control information is not information indicating a destination of the processed data. For this and other reasons, neither the data nor the control information is, or is part of, a message as recited in claim 7. Therefore, because the coprocessor 202 does not generate a message, it does not and cannot provide the message to an external source (even if one considers the processor 201 an external source). Similar analyses apply to Morikawa's coprocessors 102 (FIG. 1) and 302 (FIG. 10).

In addition to Morikawa failing to teach or suggest all of the limitations of claim 7, a convincing reason to modify Morikawa to result in the subject matter of claim 7 has not been provided. The processor 201 controls the operation of the coprocessor 202, and provides instructions to the coprocessor 202 via the bus 126 about where to send the processed data. There is no reason to modify and re-engineer the system shown in Morikawa so that the coprocessor 202 generates a message header that includes destination information. Such a modification would be contrary to the teachings of Morikawa in which the processor 201 controls the operation of the coprocessor 202 and would appear to make the system far more complex.

Claim 8

Claim 8 is patentable for reasons similar to those discussed above in support of the patentability of claim 7.

Claim 9

Claim 9 is patentable at least for reasons similar to those discussed above in support of the patentability of claim 7. For example, Morikawa fails to teach or suggest an output-data handler operable to generate a second header having first information indicating a destination of the processed data and to generate a second message that includes the processed data and the second header. Additionally, as previously discussed, there is no reason to modify Morikawa so that the coprocessor 202 generates a message that includes a header having information indicating a destination for processed data.

Claim 10

This claim is patentable by virtue of depending from claim 9.

Claim 44

Claim 44 is patentable at least for reasons similar to those discussed above in support of the patentability of claims 7 and 9.

Claims 45 and 49

These claims are patentable by virtue of their respective dependencies from claim 44.

Claim 69

Claim 69 is patentable by virtue of depending from claim 7.

Claim 70

Claim 70 is patentable by virtue of depending from claim 69.

Claim 73

Claim 73 is patentable by virtue of depending from claim 9.

Rejection Of Claims 2, 3, 12, and 15 Under 35 U.S.C. § 103(a) As Being Unpatentable Over The Respective Combinations Of References Cited In The Office Action

These claims are patentable by virtue of their respective dependencies from claims 1 and 9.

CONCLUSION

In view of the foregoing, claims 1-16, 41-50, and 66-85 are in condition for allowance. Therefore, the issuance of a formal Notice of Allowance at an early date is respectfully requested.

In the event additional fees are due as a result of this amendment, payment for those fees has been enclosed in the form of a check. Should further payment be required to cover such fees you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

Respectfully submitted,

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